IN THE CLAIMS

Please amend claims 1, 14, 16 and 18 as indicated below.

1. (Currently Amended) A coprocessor interface between a central processing unit (CPU) and a coprocessor, the interface comprising:

an instruction transfer signal group for transferring a plurality of instruction types from the CPU to the coprocessor; and

a busy signal group, coupled to said instruction transfer signal group, for signaling said instruction transfer signal group when one or more of said plurality of instruction types cannot be transferred;

wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types;

wherein said instruction transfer signal group is configured to transfer two or more of said plurality of instruction types from the CPU to the coprocessor, in parallel;

wherein said two or more of said plurality of instruction types that are transferred in parallel ~~may be~~ are of a same type ~~or of a different type~~.

2. (Original) The coprocessor interface as recited in claim 1 wherein the coprocessor comprises:

A Floating-Point Coprocessor; or

A 3-D Graphics Accelerator.

3. (Original) The coprocessor interface as recited in claim 1 wherein said plurality of instruction types comprise:

arithmetic instructions; and

data transfer instructions.

4. (Original) The coprocessor interface as recited in claim 3 wherein said data transfer instructions comprise:

TO Coprocessor data transfer instructions; and

FROM Coprocessor data transfer instructions.

5. (Original) The coprocessor interface as recited in claim 1 wherein said instruction transfer signal group comprises:

an instruction signal group, for carrying said plurality of instruction types from the CPU to the coprocessor; and

a plurality of strobe signals, each associated with a different one of said plurality of instruction types.

6. (Original) The coprocessor interface as recited in claim 5 wherein when one of said plurality of instruction types is dispatched on said instruction signal group, its transfer is completed by assertion of an associated one of said plurality of strobe signals.

7. (Original) The coprocessor interface as recited in claim 1 wherein said busy signal group comprises:

an arithmetic busy signal; and

a data transfer busy signal group.

8. (Original) The coprocessor interface as recited in claim 7 wherein said data transfer busy signal group comprises:

a TO Coprocessor data transfer busy signal; and

a FROM Coprocessor data transfer busy signal.

9. (Original) The coprocessor interface as recited in claim 1 wherein when said busy signal group stops signaling said instruction transfer group that said one or more of said plurality of instruction types cannot be transferred,

said instruction transfer group begins transfer of those instruction types, if necessary.

10. (Cancelled).

11. (Previously Presented) The coprocessor interface as recited in claim 1 further comprising:

an instruction order signal group, coupled to said instruction transfer signal group, for indicating to the coprocessor a relative execution order for said two or more of said plurality of instruction types that are transferred in parallel.

12. (Original) The coprocessor interface as recited in claim 11 wherein said two or more of said plurality of instruction types that are transferred in parallel comprise:

an arithmetic instruction; and

a data transfer instruction.

13. (Cancelled).

14. (Currently Amended) A computer program product for use with a computing device, the computer program product comprising:

a computer usable storage medium, having computer readable program code embodied in said medium, for causing a coprocessor interface to be described, said computer readable program code comprising:

first program code for providing an instruction transfer signal group for transferring a plurality of instruction types from a CPU to a coprocessor; and

second program code for providing a busy signal group when one or more of said plurality of instruction types cannot be transferred;

wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer

signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types;

wherein said instruction transfer signal group is configured to transfer two or more of said plurality of instruction types from the CPU to the coprocessor, in parallel;

wherein said two or more of said plurality of instruction types that are transferred in parallel ~~may be~~ are of a same type ~~or of a different type~~.

15. (Original) The computer program product group, as recited in claim 14 wherein said instruction transfer signal group comprises:

an instruction signal group, for carrying said plurality of instruction types from the CPU to the coprocessor; and

a plurality of strobe signals, each associated with a different one of said plurality of instruction types.

16. (Currently Amended) A computer ~~data signal embodied in a transmission~~ readable storage medium comprising:

computer-readable first program code for providing an instruction transfer signal group for transferring a plurality of instruction types from a CPU to a coprocessor; and

computer-readable second program code for providing a busy signal group for signaling said instruction transfer signal group when one or more of said plurality of instruction types cannot be transferred;

wherein when said instruction transfer signal group receives said signaling for one or more of said plurality of instruction types, said instruction transfer signal group does not transfer those instruction types, but transfers other ones of said plurality of instruction types;

wherein said instruction transfer signal group is configured to transfer two or more of said plurality of instruction types from the CPU to the coprocessor, in parallel;

wherein said two or more of said plurality of instruction types that are transferred in parallel ~~may be~~ are of a same type ~~or of a different type~~.

17. (Cancelled).

18. (Currently Amended) The computer ~~data signal~~ readable storage medium as recited in claim 16 further comprising:

computer readable third program code for providing an instruction order signal group, coupled to said instruction transfer signal group, for indicating to the coprocessor a relative execution order for said two or more of said plurality of instruction types that are transferred in parallel.

19-31. (Cancelled).